V-Band HJFET MMIC DROs With Low Phase Noise, High Power, and Excellent Temperature Stability

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***Abstract*—This paper describes the development, along with detailed phase-noise analysis, of V-band monolithic-microwave integrated-circuit (MMIC) dielectric-resonator oscillators (DROs) achieving state-of-the-art performances. A $TE_{01\delta}$-mode $Ba(Mg,Ta)O_3$ cylindrical dielectric resonator (DR) is directly placed on a MMIC GaAs substrate to avoid the loss and uncertainty of bonding wires. A 0.15-μm AlGaAs–InGaAs heterojunction field-effect transistor with optimized structure is developed as an active device. A design procedure proposed by the authors is employed, which allows us to analyze and optimize circuits in consideration for the output power, phase noise, and temperature stability. A developed DRO co-integrated with a buffer amplifier exhibits a low phase noise of −90 dBc/Hz at 100-kHz offset, a high output power of 10.0 dBm, and an excellent frequency stability of 1.6 ppm/°C at an oscillation frequency of 59.6 GHz, all of which are state-of-the-art performances reported for MMIC DROs above V-band. An experimental and theoretical analysis for the phase-noise-reduction effect of a DR is also addressed.**

***Index Terms*—Dielectric resonator oscillators (DROs), dielectric resonators (DRs), field-effect transistors (FETs), millimeter wave, monolithic microwave integrated circuits (MMICs), oscillators.**

I. Introduction

Dielectric resonator oscillators (DROs) have been demonstrated at the microwave frequency range [1]–[40] and millimeter-wave frequency range below Q-band [41], [43], [49], [52] and incorporated in various radar [18] and communication systems [2], [4], [5]. They have exhibited excellent phase-noise performance and temperature stability due to an extremely high unloaded Q factor and a small and controllable temperature coefficient of dielectric resonators (DRs) [54], [55].

Also in the frequency range above V-band, several studies have been made in recent years. 50- and 66-GHz MESFET DROs [42], a 58-GHz SiGe HBT push–push DRO [50], a 62-GHz heterostructure field-effect transistor (HFET) monolithic-microwave integrated-circuit (MMIC) DRO [47], an 81-GHz HFET DRO [48], a 93-GHz Gunn diode DRO [51], and a 98-GHz Gunn diode DRO [53] have been demonstrated. However, several problems to be solved seem to remain.

First, most of these studies [42], [50], [48], [51], [53] have been realized in the hybrid configuration (HIC) with the use of wire or flip-chip bonding techniques. In such configuration, assembly tolerances are extremely tight and can substantially affect RF performance. Hence, they are not suitable for high consumer applications. Second, none of these studies have simultaneously accomplished excellent output-power, phase- noise, and temperature-stability performances, all of which are important properties for applications of DROs. Third, the phase-noise-reduction effect of the DR is an important problem and has to be studied to verify the accuracy of design procedures (especially that of the DR model) and to obtain useful insight into the complicated mechanism of phase-noise reduction in DROs. Such analysis, however, has not been presented, even if the studies below Q-band are concerned, except a simple experimental study of Barth [51]. The second and third problems, in our opinion, are attributed primarily to the fact that small-signal-design methods have been frequently adopted [47], [48], which cannot account for such large-signal characteristics as the output power, phase noise, and temperature stability.

This paper firstly reports on MMIC DROs that simultaneously achieve low phase noise, high output power, and high temperature stability at the frequency range above V-band. A fully monolithic configuration is adopted to avoid the loss and uncertainty of bonding wires in the millimeter-wave band. A heterojunction field-effect transistor (HJFET) [also known as a high electron-mobility transistor (HEMT)] with an optimized structure is developed as an active device. An originally proposed design method [56] is employed to analyze and optimize circuits in consideration for the large-signal characteristics including temperature stability. We also address an experimental and theoretical analysis on the phase-noise-reduction effect of the DR. The analysis is accomplished by adopting a newly proposed circuit configuration, which allows oscillation at almost the same frequency for two states, i.e., "DR-stabilized" (with DR) and "DR-unstabilized" (without DR).

II. Monolithic Resonant Structure

In most of the previous studies, DROs were realized in HIC utilizing a ceramic circuit substrate. A partially monolithic configuration was also adopted by several authors [4], [13], [15], [21], [23], [28], [43], [49], where an oscillator circuit excluding a resonant circuit was monolithically integrated and a DR was put on an external ceramic substrate. In these configurations, bonding wires are required to connect an active-device chip with the circuit substrate or a monolithic oscillator chip with the

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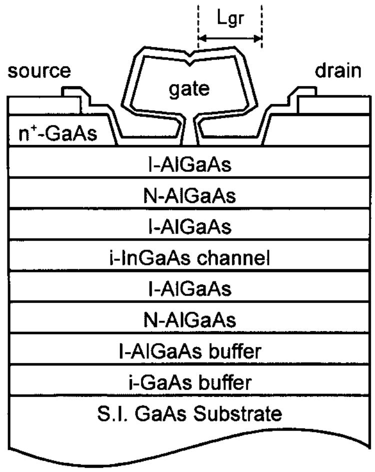


Fig. 1. Cross-sectional view of an AlGaAs–InGaAs HJFET with a gate length of 0.15 μm.

external resonant circuit. However, in the millimeter-wave range, bonding wires are lossy and difficult to characterize. Thus, a fully monolithic configuration [11], [12], [45]–[47] is preferable and adopted in this study, where a DR is placed directly on a GaAs MMIC chip and is coupled to a microstrip line (MSL) fabricated on the same substrate. A cylindrical resonator, made of Ba(Mg, Ta)O_3 whose relative dielectric constant is 23.8, is adopted. The cross-sectional view of the resonant structure is shown in [56]. An unloaded Q factor of the resonant structure is approximately 2000 (that of the DR itself is approximately 5000) [57].

This monolithic resonant structure (the DR coupled to an MSL on GaAs) is modeled as an originally proposed *RLC* parallel resonant circuit [57]. One of the notable features of our model is that equivalent-circuit parameters ($R, L,$ and C) are represented as a function of the ambient temperature and structural parameters (the airgap between the DR top surface and a tuning screw, and the distance between the DR and MSL). A detailed derivation procedure for this model is described in [57]. This model is introduced in a harmonic-balance (HB) circuit simulator to optimize circuit parameters, including a temperature coefficient of the DR and structural parameters, in consideration of various DRO performances such as the oscillation frequency, output power, and phase noise [56].

III. Design and Modeling of Heterojunction Field-Effect Transistor (HJFET)

To realize MMIC DROs with high output power at such a high frequency range as V-band, an active device with excellent high-frequency characteristics and high-power deliverability has to be developed. We developed an AlGaAs–InGaAs HJFET [58] with an optimized device structure.

The cross-sectional view of the device is shown in Fig. 1. The active part of the epitaxial layer structure consists of an undoped InGaAs channel layer sandwiched between two heavily doped n-type AlGaAs layers. An undoped AlGaAs layer was used as a Schottky contact layer. A 0.15-μm T-shaped Ti–Al–Ti gate was fabricated by an electron-beam evaporation and liftoff technique [59].

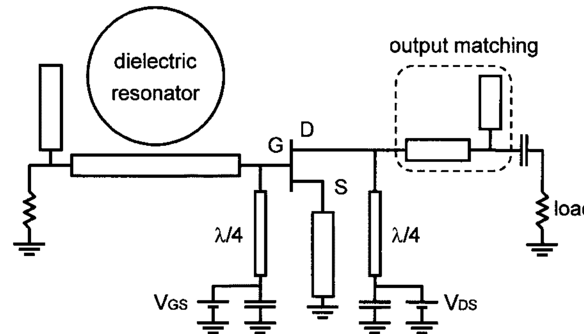


Fig. 2. Circuit schematic of 55-GHz-band HJFET DRO.

The recess distance from the gate to the drain edge ($L_{\rm gr}$) is an important parameter that has strong effects on both dc and high-frequency performances. We experimentally optimized this parameter to be 0.4 μm considering both the maximum stable gain (MSG) at 60 GHz for high-frequency operation and the maximum drain current ($I_{\rm max}$) for high-power performance [58]. As a result, the maximum oscillation frequency ($f_{\rm max}$) of 230 GHz and $I_{\rm max}$ of 40 mA were obtained for the optimized HJFET with 100-μm gatewidth. These performances show that the optimized HJFET has great potential as an active device for millimeter-wave oscillator and amplifier applications.

The HJFET was modeled using the Curtice cubic model [60] to carry out nonlinear oscillator analyses. As detailed in [56], this model was further modified to be dependent on temperature. It, in conjunction with the temperature dependent DR model [57] mentioned in Section II, allows us to optimize a circuit and to select a DR with an appropriate temperature coefficient considering temperature stability of DROs [56].

IV. Design, Analysis, and Performances of DROs

A. Circuit Design and Fabrication

As a prototype for a 60-GHz-band frequency source described in Section IV-E, a 55-GHz-band HJFET MMIC DRO [44] was designed, fabricated, and analyzed. A novel circuit configuration was employed to achieve oscillation at approximately the same frequency for the two states, i.e., the DR-stabilized state (with a DR) and the unstabilized state (without a DR). This allows direct experimental analyses for the phase-noise-reduction effect of the DR.

Fig. 2 illustrates the circuit schematic of the DRO. The DRO consists of a series feedback topology with a 100-μm gatewidth HJFET in a common-source configuration. The resonant circuit, composed of a $\rm TE_{01\delta}$-mode Ba(Mg,Ta)O_3 cylindrical DR coupled to an MSL, is connected to the gate terminal of the HJFET. The MSL is generally terminated by a resistor whose resistance is equal to the characteristic impedance of the MSL. In this study, however, the MSL is terminated with a parallel combination of a resistor and a quarter-wavelength open stub. Adopting such a circuit configuration makes it possible to satisfy the oscillation condition at almost the same frequency in the two states, i.e., with and without a resonator. Fig. 3(a) and (b) illustrates the equivalent circuit of the DRO with and without a DR, respectively. The "device-circuit impedance" $Z_G(\varepsilon, A, \omega)$

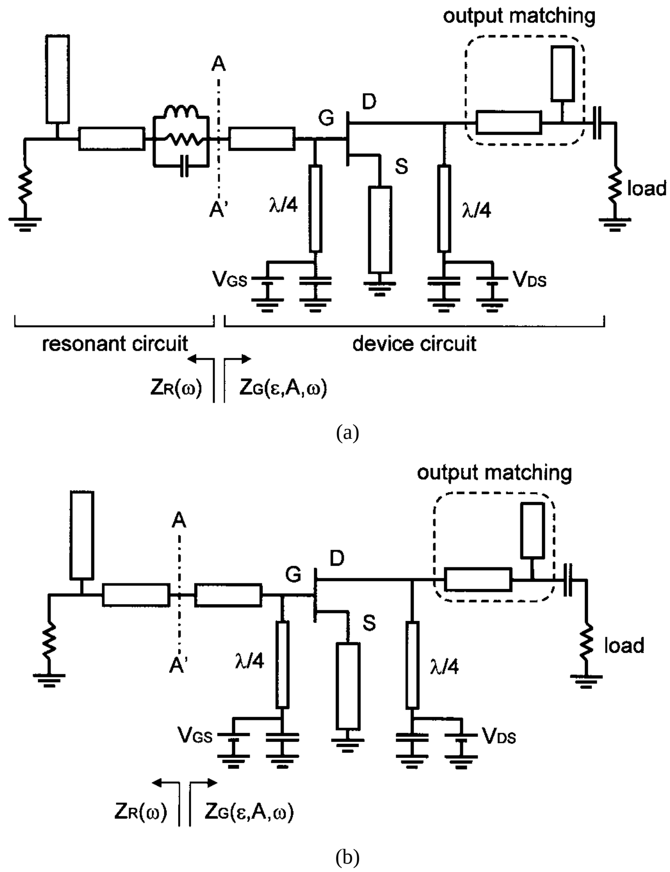


Fig. 3. Equivalent circuits for a 55-GHz-band DRO. (a) DR-stabilized state (with a DR). The DR coupled to an MSL in Fig. 2 is replaced by an *RLC* parallel resonant circuit. (b) Unstabilized state (without a DR). The *RLC* parallel resonant circuit in (a) is removed.

and the "resonant-circuit impedance" $Z_R(\omega)$ are defined in this figure. Here, ε denotes a modulation source, which is usually $V_{\rm gs}$ for FET-type devices [61], [62]. A parameter A represents an oscillation amplitude, and ω is an angular frequency. These parameters at an operation point are denoted as $(\varepsilon_0, A_0, \omega_0)$.

On the circuit design, circuit parameters, including the structural parameters of the resonant structure and the temperature coefficient of the DR, were optimized in consideration of not only oscillation frequency, but of output power, phase noise, and temperature stability based on the design method proposed by the authors [56]. In [56], we demonstrated that our design method well predicts temperature- and structural-parameter-dependent characteristics of DROs. In this paper, our design method will be further verified through analyses on the phase-noise-reduction effects of the DR (Sections IV-B–D), as well as a demonstration of excellent DRO performances (Sections IV-E and F).

The photograph of the fabricated MMIC DRO with a DR directly placed on the MMIC chip is shown in Fig. 4. Metal–insulator–metal (MIM) capacitors, epitaxial layer resistors, air bridges, and via-holes were employed for monolithic integration.

In Sections IV-B–D, we will discuss the effects of the DR on circuit impedance, pushing figure, and phase noise of the DRO based on analytical calculations, numerical (HB) simulations, and experiments.

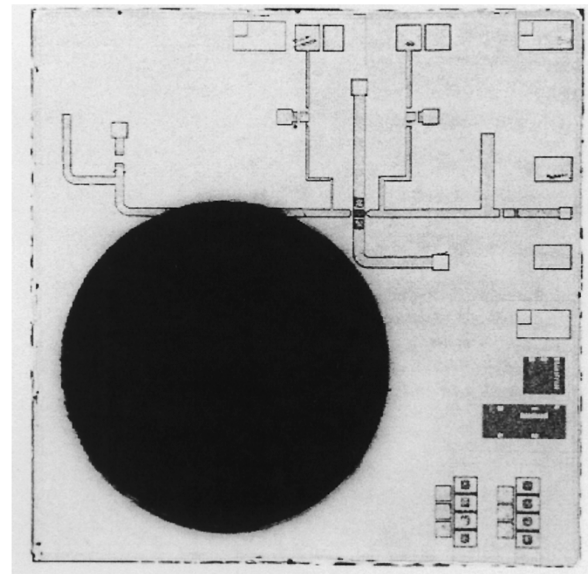


Fig. 4. Topside view of the 55-GHz-band HJFET MMIC DRO with a cylindrical DR of diameter 1.3 mm (chip size: 2.22 mm × 2.22 mm).

B. Circuit Impedance Analysis

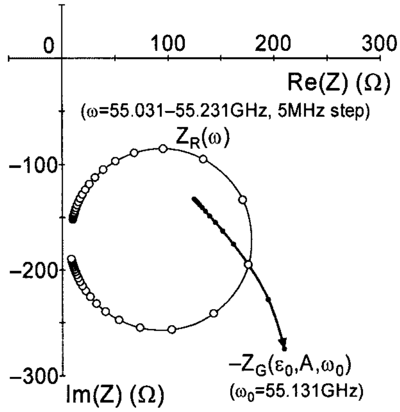
In this section, we analyze circuit impedances and predict effects of the DR on the pushing figure and phase noise based on analytical expressions. By doing so, we can obtain some insight into the complicated mechanism of phase-noise reduction in DROs.

Fig. 5(a) and (b) plots the calculated device-circuit impedance $-Z_G(\varepsilon_0, A, \omega_0)$ with A as a parameter and the resonant-circuit impedance $Z_R(\omega)$ with ω as a parameter for the DR-stabilized and DR-unstabilized states. These are computed by HB and linear-circuit analyses. Here, $-Z_G(\varepsilon_0, A, \omega_0)$ for two states are not identical with each other because angular oscillation frequency ω_0 is slightly different. As can be seen from these figures, frequency sensitivity of $Z_R(\omega)$ is dramatically improved by adopting the DR. Values of $|dZ_R/d\omega|_{\omega_0}$ for the two states are listed in the first row of Table I. The improvement is by a factor of 249.

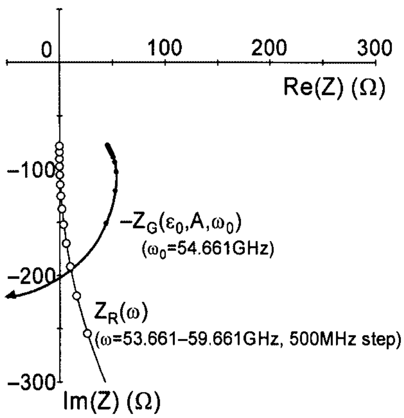
According to Kurokawa's theory [63] for negative-resistance oscillator noise, which was later expanded by Riddle and Trew [61], the spectral density of the flicker-FM noise [64], $S_{\phi_f}(\omega_m)$ can be written as

$$S_{\phi_f}(\omega_m) = \frac{\delta\varepsilon^2(\omega_m)}{\omega_m^2} \cdot \frac{A_0^2 \left|\frac{\partial Z_t}{\partial \varepsilon} \times \frac{\partial Z_t}{\partial A}\right|^2_{\varepsilon_0, A_0, \omega_0} + \omega_m^2 \left|\frac{\partial Z_t}{\partial \varepsilon} \cdot \frac{\partial Z_t}{\partial \omega}\right|^2_{\varepsilon_0, A_0, \omega_0}}{A_0^2 \left|\frac{\partial Z_t}{\partial A} \times \frac{\partial Z_t}{\partial \omega}\right|^2_{\varepsilon_0, A_0, \omega_0} + \omega_m^2 \left|\frac{\partial Z_t}{\partial \omega}\right|^4_{\varepsilon_0, A_0, \omega_0}} \tag{1}$$

where $\delta\varepsilon^2(\omega_m)$ denotes the low-frequency noise of an active device and ω_m is the offset angular frequency. $Z_t(\varepsilon, A, \omega) = Z_G(\varepsilon, A, \omega) + Z_R(\omega)$ is the impedance of the whole oscillator circuit. Since measured single-sideband (SSB) phase noise had a slope of approximately ω_m^{-3} at around $\omega_m/2\pi = 100$ kHz (i.e., the phase noise is dominated by the flicker-FM noise at this offset frequency), we do not discuss the white FM noise [64] in



(a)



(b)

Fig. 5. Resonator impedance and negative of device impedance in the complex impedance plane. (a) DR-stabilized state (with a DR). (b) Unstabilized state (without a DR).

this paper. Note that SSB phase noise is approximately given by $S_{\phi_f}(\omega_m)/2$. Our numerical calculations on various DROs show that the second terms of the numerator and denominator in (1) are negligible, as compared to the first terms. Hence, (1) can be precisely approximated as follows:

$$S_{\phi_f}(\omega_m) = \frac{\delta\varepsilon^2(\omega_m)}{\omega_m^2} \cdot \frac{\left|\frac{\partial Z_t}{\partial \varepsilon}\right|^2_{\varepsilon_0, A_0, \omega_0} \sin^2\phi}{\left|\frac{\partial Z_t}{\partial \omega}\right|^2_{\varepsilon_0, A_0, \omega_0} \sin^2\theta} \tag{2}$$

where θ is the intersection angle between vectors $\partial Z_t/\partial A$ and $\partial Z_t/\partial\omega$, and ϕ is the intersection angle between vectors $\partial Z_t/\partial\varepsilon$ and $\partial Z_t/\partial A$ at an operation point $(\varepsilon_0, A_0, \omega_0)$.

Four parameters in (2), $|\partial Z_t/\partial\omega|_{\varepsilon_0,A_0,\omega_0}$, $|\partial Z_t/\partial\varepsilon|_{\varepsilon_0,A_0,\omega_0}$, $\sin\theta$, and $\sin\phi$ are calculated for the DR-stabilized and DR-unstabilized states (Table I). The frequency sensitivity of the whole circuit $|\partial Z_t/\partial\omega|_{\varepsilon_0,A_0,\omega_0}$ was improved by a factor of 34 by adopting a DR. This improvement factor is smaller than 249 for $|dZ_R/d\omega|_{\omega_0}$. It is because $dZ_G/d\omega$ cannot be neglected in comparison to $dZ_R/d\omega$ for the unstabilized state. However, the improvement is still great to decrease the pushing figure and to reduce the phase noise drastically, as described below. Changes in the other three parameters ($|\partial Z_t/\partial\varepsilon|_{\varepsilon_0,A_0,\omega_0}$, $\sin\theta$, and $\sin\phi$) are negligible as compared to the change in $|\partial Z_t/\partial\omega|_{\varepsilon_0,A_0,\omega_0}$.

The flicker FM noise spectral density (2) is associated with the pushing figure ($df_0/d\varepsilon|_{\varepsilon_0}$, where $f_0 = \omega_0/2\pi$ denotes an oscillation frequency), which is directly measurable via the following relation:

TABLE I
SIMULATED VALUES FOR PARAMETERS IN (2). RATIOS OF THESE PARAMETERS OF DR-STABILIZED AND DR-UNSTABILIZED STATES ARE ALSO SHOWN

parameter	DR-stabilized	unstabilized	ratio
$\lvert dZ_R/d\omega\rvert$ (Ω×sec/rad)	1990×10^{-9}	8×10^{-9}	249
$\lvert\partial Z_t/\partial\omega\rvert$ (Ω×sec/rad)	2052×10^{-9}	61×10^{-9}	34
$\lvert\partial Z_t/\partial\varepsilon\rvert$ (Ω/V)	433	173	2.5
$\sin\theta$	0.68	0.52	1.3
$\sin\phi$	0.36	0.45	0.8

TABLE II
PUSHING-FIGURE REDUCTION BY ADOPTING A DR (COMPARISON AMONG ANALYTICAL EXPRESSION, HB SIMULATION, AND MEASUREMENT). FLICKER FM NOISE REDUCTION VALUES CALCULATED BY AN ANALYTICAL EXPRESSION (3) USING ANALYTICALLY CALCULATED, HB-SIMULATED, AND MEASURED PUSHING FIGURES ARE ALSO LISTED

	pushing figure $\lvert df_0/d\varepsilon\rvert_{\varepsilon 0}$ (MHz/V)			flicker-FM noise reduction (dB) calculated by (3)
	DR-stabilized	unstabilized	ratio	
analytical	17.4	390	22.4	27
HB simulation	12.6	242	20.2	26
measurement	7.8	226	30.0	29

$$S_{\phi_f}(\omega_m) = \frac{4\pi^2\delta\varepsilon^2(\omega_m)}{\omega_m^2} \cdot \left|\frac{df_0}{d\varepsilon}\right|^2_{\varepsilon_0} \tag{3}$$

where

$$\left.\frac{df_0}{d\varepsilon}\right|_{\varepsilon_0} = \frac{1}{2\pi} \cdot \frac{\left|\frac{\partial Z_t}{\partial\varepsilon}\right|_{\varepsilon_0,A_0,\omega_0} \sin\phi}{\left|\frac{\partial Z_t}{\partial\omega}\right|_{\varepsilon_0,A_0,\omega_0} \sin\theta}. \tag{4}$$

The pushing figure for the two states calculated by (4) (using the values in Table I) are shown in the first row of Table II. The pushing figure decreased from 390 to 17.4 MHz/V (by a factor of 22.4) mainly due to the improvement of $|\partial Z_t/\partial\omega|_{\varepsilon_0,A_0,\omega_0}$. Substituting these pushing-figure values into (3) predicts that adopting the DR reduces the flicker FM noise by 27 dB (also shown in Table II).

C. Measurement and HB Simulation of Pushing Figure

Measured gate-bias pushing characteristics for the two states are plotted in Fig. 6 along with HB-simulation results. Measured and HB-simulated characteristics are in fair agreement with each other for both of the states. The measured pushing figure was reduced from 226 to 7.8 MHz/V (by a factor of 30.0) by adopting a DR, whereas the HB-simulated pushing figure was reduced from 242 to 12.6 MHz/V (by a factor of 20.2), as listed in Table II. These values are approximately in accord with the values predicted from the circuit-impedance analysis (listed in the first row of Table II).

Flicker FM noise reduction can be estimated from these HB-simulated or measured pushing-figure values utilizing (3).

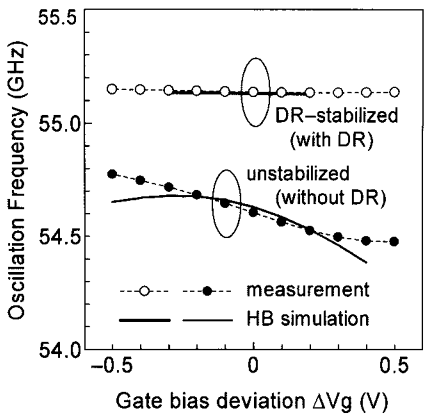


Fig. 6. Comparison of gate-bias pushing characteristics of the 55-GHz-band HJFET MMIC DRO for DR-stabilized (with a DR) and unstabilized (without a DR) states.

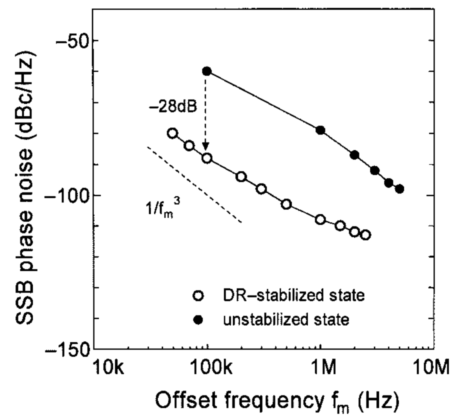


Fig. 8. Comparison of SSB phase-noise performance of the 55-GHz-band HJFET MMIC DRO for DR-stabilized (with a DR) and DR-unstabilized (without a DR) states.

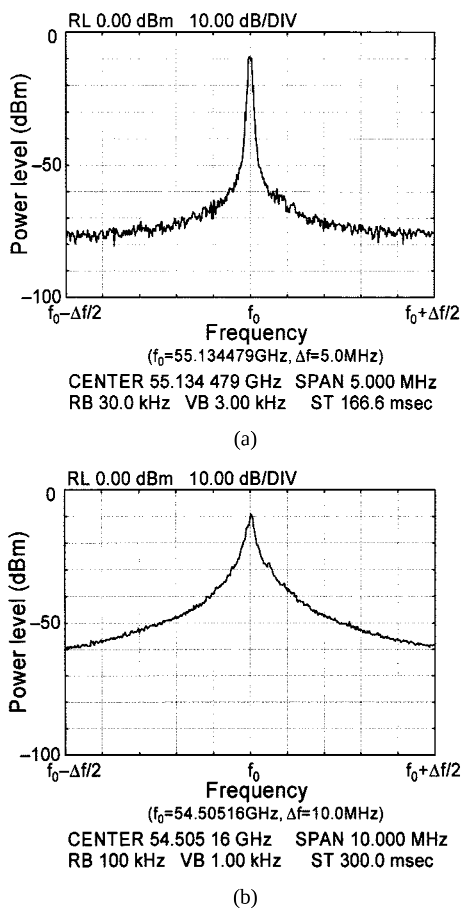


Fig. 7. Output spectrum of the 55-GHz-band HJFET MMIC DRO. (a) DR-stabilized state (with a DR). (b) DR-unstabilized state (without a DR).

Estimated values for the flicker FM noise reduction are 26 and 29 dB, respectively (also listed in Table II).

D. Measurement of Phase Noise

Fig. 7(a) and (b) demonstrates the output spectrum for the DRO in DR-stabilized and DR-unstabilized states, respectively. A stable oscillation was obtained at 55.135 GHz with an output power of 3.7 dBm when the DR was coupled to the oscillator. When the DR was removed, the oscillation frequency was 54.6 GHz, which is slightly lower than the stabilized one, with a relatively high output power of 7.6 dBm. No spurious oscillation was observed in both states.

Fig. 8 depicts measured SSB phase noise of the DRO in the DR-stabilized and DR-unstabilized states. The DRO exhibited a low phase noise of −88 dBc/Hz at 100-kHz offset in the DR-stabilized state. Measured phase-noise improvement amounts to 28 dB at 100-kHz offset.

The phase noise at this offset frequency has a slope of approximately ω_m^{-3} and is considered to be dominated by the flicker-FM noise [64]. We can, therefore, compare the measured phase-noise-reduction value with the flicker FM-noise-reduction values predicted from the analytically calculated, HB-simulated, and measured pushing figures in previous sections. The measured reduction value (28 dB) is in reasonable agreement with the predicted ones listed in Table II.

These results demonstrated in Sections IV-B–D conclude the following.

1) Our HB-based design procedure [56], featuring an original DR model [57], is able to make accurate estimates of phase-noise-reduction effects of the DR. It is, therefore, useful for accurate design of millimeter-wave DROs.
2) Analytical expressions (2) and (4) combined with circuit-impedance analyses also precisely predict reductions of the phase noise and pushing figure. Due to their analytical nature, they give some insight into the mechanism of the phase-noise reduction [an example is mentioned in 3)].
3) Phase-noise reduction is achieved mainly due to an increase in frequency sensitivity of a resonant circuit $(|dZ_R/d\omega|_{\omega_0})$. However, the effect is weakened by frequency sensitivity of a device circuit $(|\partial Z_G/\partial\omega|_{\varepsilon_0,A_0,\omega_0})$, which cannot be neglected in the millimeter-wave range.

To the authors' knowledge, the analyses and experiments described in Sections IV-B–D are the first attempt to discuss the phase-noise-reduction effects of a DR in DROs through comparative experiments along with theoretical calculations. Our design procedure [56], whose accuracy is thus verified, is utilized to realize a 60-GHz-band frequency source in Section IV-E.

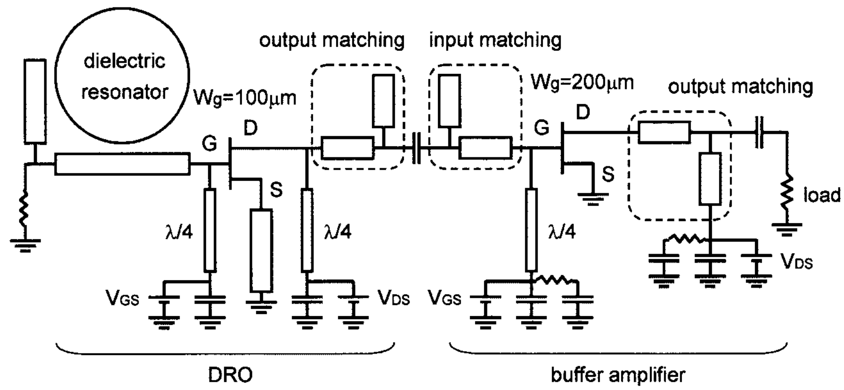


Fig. 9. Circuit schematic for 60-GHz-band HJFET MMIC DRO co-integrated with a buffer amplifier.

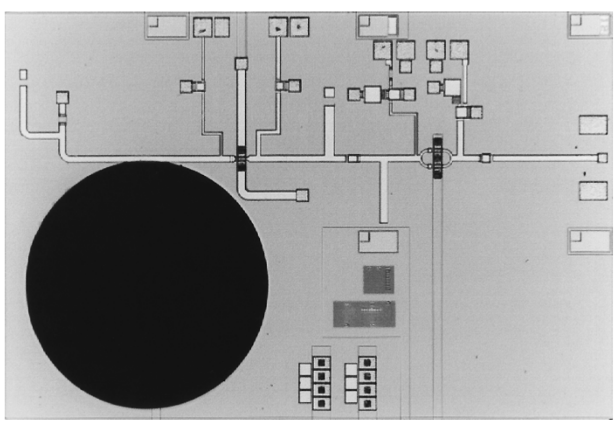


Fig. 10. Photograph for the 60-GHz-band HJFET MMIC DRO co-integrated with a buffer amplifier. Chip size: 2.22 mm × 3.37 mm.

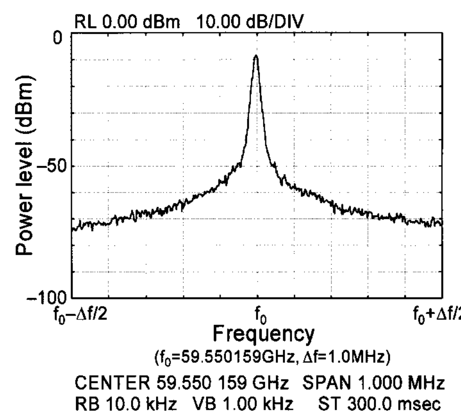


Fig. 11. Typical output spectrum for the 60-GHz-band HJFET MMIC DRO co-integrated with a buffer amplifier. The MMIC was assembled in a metal package with a microwave integrated circuit (MIC)/waveguide transition. The output power of the MMIC was divided by a directional coupler between a spectrum analyzer and a power meter for the evaluation of the oscillation spectrum and output-power level, respectively. (The output power of the MMIC itself was +10 dBm.)

E. Development of a V-Band DRO Co-Integrated With Buffer Amplifier

The final purpose of this study is to develop a signal source with low phase noise, high output power, and excellent temperature stability at the 60-GHz band. We designed a 60-GHz-band MMIC DRO co-integrated with a buffer amplifier [65] based on the proposed design method [56] whose accuracy was further verified in Sections IV-B–D. Fig. 9 illustrates the circuit schematic. The oscillator has the same circuit configuration as described in Section IV-A. The amplifier employs the HJFET with 200-μm gatewidth to deliver a high output power. The input matching circuit consists of a transmission line and an open stub, while the output matching circuit consists of a transmission line and a short stub. *R–C* networks are adopted in the bias circuit to suppress parasitic oscillations. Circuit parameters, structural parameters of the resonant structure, and the temperature coefficient of the DR were optimized by the proposed design method [56] considering all respects of output power, phase noise, and temperature stability. The chip photograph for the fabricated MMIC DRO with a cylindrical DR is shown in Fig. 10. Fig. 11 shows a typical output spectrum of the DRO. Stable oscillation was obtained at the oscillation frequency of 59.6 GHz. The DRO exhibited a low phase noise of −90 dBc/Hz at 100-kHz offset, a high output power of 10.0 dBm, and an excellent temperature stability of 1.6 ppm/°C. These performances are sufficient for applications to various high-quality communication systems.

F. Summary of Performances

Fig. 12(a)–(c) summarizes the phase-noise (at 100-kHz offset), output-power, and temperature-stability performances reported for microwave and millimeter-wave DROs [1]–[53] based on various active device technologies. Performances of the 55-GHz DRO (denoted as "this work (A)") and the 60-GHz DRO with a buffer amplifier (denoted as "this work (B)") demonstrated in this study are also plotted. The DROs developed in this study benchmark the best performances in all respects of phase noise, output power, and temperature stability so far as MMIC DROs above V-band are concerned. Even if hybrid DROs are included, this is believed to be the first report for the DRO that simultaneously achieves excellent phase-noise, output-power, and temperature-stability performances above V-band. These results confirm the validity of our design and analysis method [56] featuring original DR and HJFET models.

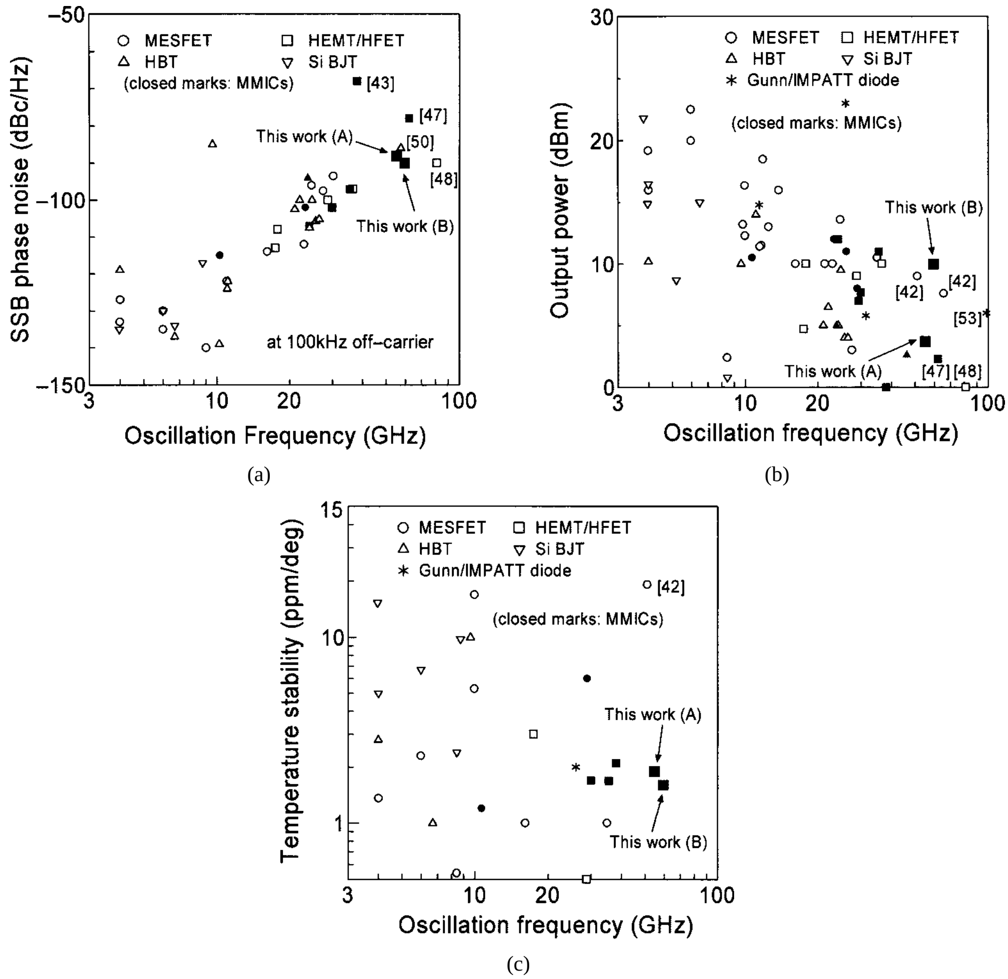


Fig. 12. Summary of previously reported DRO performances based on various device technologies: MESFET [1]–[18], [41], [42], HEMT [19]–[23], [43]–[45], HFET [47], [48], HBT [24]–[33], [49], [50], Si bipolar junction transistor (BJT) [34]–[38], and Gunn/IMPATT diode [39], [40], [51]–[53]. Closed marks denote MMICs (diode-based DROs are all in HIC). Performances of 55-GHz DRO (A) and 60-GHz DRO (B) demonstrated in this study are also plotted. (a) SSB phase noise at 100-kHz offset. (b) Output power. Note that the DRO of this study (B) is integrated with a buffer amplifier. As the amplifier has a gain of approximately 7 dB, the output power of the 60-GHz DRO itself is calculated as 3 dBm. (c) Temperature stability.

V. Conclusion

We have demonstrated V-band MMIC DROs that benchmark the state-of-the-art performances in all respects of phase noise, output power, and temperature stability among reported MMIC DROs above V-band. A MMIC technology based on a 0.15-μm AlGaAs–InGaAs HJFET with an optimized device structure was developed. A fully monolithic configuration was adopted to avoid the use of bonding wires. A design procedure proposed by the authors was employed to optimize circuits in consideration of output power, phase noise, and temperature stability. A 60-GHz-band MMIC DRO co-integrated with a buffer amplifier was designed and fabricated based on the above-mentioned design and fabrication technologies. It exhibited a low phase noise of -90 dBc/Hz at 100-kHz offset, high output power of 10.0 dBm, and an excellent temperature stability of 1.6 ppm/°C at an oscillation frequency of 59.6 GHz.

We have also addressed an analysis for the phase-noise-reduction effect of a DR in DROs. A new circuit configuration has been employed to obtain oscillation at the same frequency for two states: with and without a DR, which allows direct experiments on the phase-noise-reduction effect of the DR. Good agreement between experimental and theoretical results for the effect confirmed accuracy of our design method. The analysis also gave some insight into the complicated mechanism of the phase-noise-reduction effect of the DR.

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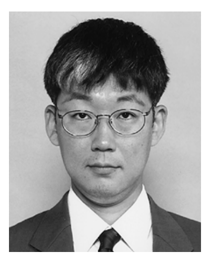

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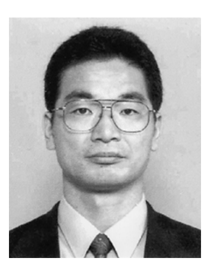

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